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10/619,136

PATENT

Conf. No. 6066

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: David Mark et al.

Assignee: Xilinx, Inc.

Title: "Method for Gross I/O Functional Test at Wafer Sort"

Serial No.: 10/619,136

Filing Date: 07/14/2003

Examiner: Jimmy Nguyen

Art Unit: 2829

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RESPONSE TO THE SECOND OFFICE ACTION

In response to the Second Office Action mailed from the Patent Office on December 30, 2004, Applicants submit a terminal disclaimer and the following remarks.

Claims 1, 3-18, and 20-26 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-17 of U.S. Patent No. 6,788,095. In response, Applicants submit herewith a terminal disclaimer for the present invention with respect to the cited patent. Therefore, Applicants respectfully request withdrawal of the rejection and allowance of claims 1, 3-18, and 20-26.

Reconsideration and a notice of allowance are respectfully requested in view of the remarks presented above. If the Examiner has any questions or concerns, a telephone call to the undersigned is invited.

Respectfully submitted,

Justin Liu  
Attorney for Applicants  
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I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patents, P.O. BOX 1450, Alexandria, VA 22313-1450, on March 24, 2005.

Julie Matthews  
Name

  
Signature